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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/572,691	01/05/2007	Jean-Raphael Bezal	PF030152	4984

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EXAMINER	
SIM, YONG H	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
11/02/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/572,691	BEZAL ET AL.	
	Examiner	Art Unit	
	YONG H. SIM	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-11* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-11* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1 – 11 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. **Claims 1 – 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Awamoto (US 6,369,514 B2) in view of Velayudhan et al. (Hereinafter "Velayudhan" US 6,917,351 B1).**

Regarding claim 1, Awamoto teaches Device for driving a plasma display panel having a plurality of cells arranged in rows and, the rows of cells being distributed in a plurality of block of lines columns (See Fig. 1. Y, X and A. Also see Fig. 2. See Fig. 8 for blocks of lines of columns 781.), said device comprising row address means for selectively addressing the display cell rows within the blocks and creating, where required, in cooperation with means for selectively applying data voltages to the display columns, an electrical discharge inside the cell disposed at the intersection of the row and column selected during an address phase (Col. 8, lines 20 – 27; "The Y driver includes a scanning circuit and a common driver. The address driver controls the potential of the total m of third electrodes A in accordance with the subfield data Dsf."), and sustain means (791 "sustain circuit" Fig. 8) for sustaining the electrical discharges inside said cell during a sustain phase immediately following the address phase (See Col. 1, lines 51 – 56; "when increasing the sustaining voltage Vs, the cell voltage exceeds the discharge start voltage .. so that the surface discharge occurs …" Also see Fig. 11 for the sustain period immediately following the address period. Col. 8, lines 62 – 67; "In the display, the period of one subfield includes a reparation period TR, an

address period TA and a sustaining period TS in the same way as the conventional driving method (see Fig. 11)."), wherein said in that said row address means comprise separate row address means for each said block of rows addressing successively the blocks of rows by applying a first voltage to the cells of the selected block (Col. 9, lines 10 – 15; "In the first half … the selected row is biased to a selection potential Vya1.") and a second voltage to the cells of the other blocks, said second voltage being greater than the first voltage (Col. 9, lines 10 – 15; "The second electrodes that are not selected in this period are all biased to a second non-selection potential Vya3... Vaa<Vya3<Vya2<Vya1 is satisfied.") and said row address means and/or sustain means are capable of allowing a bi-directional current to flow within the cells of the display during said address and/or sustain phases (Col. 10, line 53 – Col. 11, line 4; "supplies the sustaining pulse to the positive polarity and the power source terminals SU, SD when being biased to the negative potential … all the second electrodes $Y_{(n/2)+1}$ – Y_n are connected to the ground bi-directional so as to be the ground potential."), said separate row address means comprising:

at least one row driver circuit for each of the blocks of rows (781 "scanning drivers" Fig. 8) connected between the first and second connection lines (See Fig. 1, SU is a first connection lines and SD is a second connection lines.) and designed to apply, during an address phase specific to said block of rows, the potential of one of said first and second connection lines to a first electrode of the cells of a plurality of rows of the block (Col. 10, lines 58 – 63; "… the sustaining circuit that supplies the

sustaining pulse of the positive polarity and the power source terminals SU, SD when being biased to the negative potential."),

a first switch ($Q5_1$ "switch" Fig. 8);

a second switch ($Q6_1$ "switch" Fig. 8) for selectively applying an address voltage to the second connection line during the address phase (See Fig. 8),

a first diode connected to the common point of the first switch and of the capacitor for supplying the first voltage (See Fig. 8. a diode is connected to $Q5_1$ to apply the first potential Vya.)

But Awamoto does not expressly describe a capacitor, a first terminal of which being coupled to the first connection line via a first switch and a second terminal which being coupled to the second connection line;

However, in a similar field of endeavor, Velayudhan teaches an energy recovery for a PDP comprising a capacitor, a first terminal of which is being coupled to a first connection line via a first switch and a second terminal being coupled to a second connection line (See Fig. 6a. There are plurality of capacitors in the figure of which one terminal of the capacitor is connected to a connection line to a first switch and the other to a second connection line.)

Therefore, it would have been obvious to a person having ordinary skill in the art to incorporate the idea of having a capacitor, a first terminal of which is being coupled to a first connection line via a first switch and a second terminal being coupled to a second connection line as taught by Velayudhan into the device as taught by Awamoto to obtain a device for driving a plasma display panel having a capacitor, a first terminal of which

is being coupled to the first connection line via a first switch and a second terminal of which is being coupled to the second connection line to conserve energy by providing a recovery circuit.

Regarding claim 2, Awamoto as modified above teach the device according to claim 1, wherein the separate row address means for each block of rows further comprises:

a switching means for isolating said first connection line from the sustain means of said driver device during the row address phase of the relevant block (Col. 10, lines 65 – 67; “a switch is turned on for flowing the current to the ground in the sustaining circuit …”), and a third switch ($Q8_1$ “switch” Fig. 8) for applying said second voltage to said first connection line during the address phases specific to the other blocks (See Fig. 8 and Col. 10, lines 53 – 67).

Regarding claim 3, Awamoto as modified above teach the device according to claim 2, wherein said third switch is common to the address means of the blocks of rows (See Fig. 8).

Regarding claim 4, Awamoto as modified above teach the device according to claim 3, wherein the switching means is a switch connected between the sustain means of the device and said first connection line, which switch is open during the row address

phase of the relevant block (See Fig. 13 for the detailed switch connection of sustaining circuits. Also see Col. 10, lines 53 – 67.).

Regarding claim 5, Awamoto as modified above teaches device according to claim 2, wherein said second voltage is equal to a high sustain voltage (A high sustain voltage can be any voltage that is equal to the second voltage which is Vya3).

Regarding claim 6, Awamoto as modified above teaches a device according to claim 2, wherein the sustain means comprise: third and fourth switches (See Fig. 13 for the third switch which is connected to SU and the fourth switch which is connected to SD) for selectively applying a high sustain voltage and a low sustain voltage to said first connection line of the blocks when the switching means of said blocks is in the on state (Col. 10, lines 58 – 63; "… the sustaining circuit that supplies the sustaining pulse of the positive polarity and the power source terminals SU, SD when being biased to the negative potential.), fifth and sixth switches for selectively applying said high sustain voltage and said low sustain voltage to a second electrode of the cells of the plurality of rows selected by said row driver circuit (See Fig. 8, Fig. 8 shows two identical sustaining circuits which comprises fifth and sixth switches. Also see Col. 10, lines 58 - 63), said third and sixth switches on the one hand, and said fourth and fifth transistors on the other, being controlled in an identical manner (Since the sustaining circuits are equivalent, they will be controlled in an identical manner.).

Regarding claim 7, Awamoto as modified above teaches a device according to claim 6, wherein the sustain means additionally comprise: a second diode connected in series with said third switch and oriented so as to allow a current to flow into the first connection line of the blocks when the switching means of said blocks is in the on state (See Fig. 8, a diode is serially connected between the sustaining circuit and a switch to allow a current to flow in the first connection line SU) , and third and fourth diodes connected in parallel with the third and fourth switches respectively, and fifth and sixth diodes connected in parallel with the fifth and sixth switches, respectively (See third and fourth diodes within the sustaining circuit 790 in Fig. 13. The fifth and sixth diodes would be connected in the same manner in the second sustaining circuit as shown in Fig. 8).

Regarding claim 8, Awamoto as modified above teaches a device according to claim 3, wherein said third switch is connected in parallel with a second diode (See Fig. 8 for the parallel configuration.).

Regarding claim 9, Awamoto as modified above, teaches a device according to claim 6, wherein the sustain means additionally comprise a fifth switch inserted between the first and second connection lines of each block, which switch is open during the row address phase of the relevant block and closed during the sustain phase (See Fig. 13. The sustaining circuit shows a power recovering circuit comprising switches which are

inserted between the first and second connection lines which would be open during the row address phase.).

Regarding claim 10, Awamoto, as modified above, teaches a device according to claim 9, in addition Velayudhan teaches, wherein the switching means for isolating the first connection line from the sustain means of said driver device during the row address phase of the relevant block comprises a seventh diode connected between the sustain means of the device and said first connection line, which diode is oriented so as not to allow a current to flow in the direction of the first connection line (See Fig. 6a there are a couple of diodes which prevents the flow of current towards a connection lines.) and in that the fifth switch is inserted between the sustain means of the device and said second connection line (Awamoto: See Fig. 13, the fifth switch is inserted between the sustain means of the device and the second connection line SD).

Regarding claim 11, Awamoto as modified above teaches a plasma display panel wherein it comprises a driver device according to claim 1 (See Col 7, lines 46 – 65).

Conclusion

1. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YONG H. SIM whose telephone number is (571)270-1189. The examiner can normally be reached on Monday - Friday (Alternate Fridays off) 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/YONG H SIM/
Primary Examiner, Art Unit 2629
10/25/2011